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JC955 U.S. PTO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventorship Sidiropoulos et al.
Applicant Rambus Inc.
Attorney's Docket No. RB1-005US
Title: Reducing Coupled Noise in Pseudo-Differential Signaling Systems

JC688 U.S. PTO
09/708795
11/07/00

TRANSMITTAL LETTER AND CERTIFICATE OF MAILING

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231
From: Daniel L. Hayes (509) 324-9256
Lee & Hayes, PLLC
421 W. Riverside Avenue, Suite 500
Spokane, WA 99201

The following enumerated items accompany this transmittal letter and are being submitted for the matter identified in the above caption.

- 1. Transmittal Letter with Certificate of Mailing included.
- 2. PTO Return Postcard Receipt
- 3. Check in the Amount of \$1,916
- 4. Fee Transmittal
- 5. New patent application (title page plus 31 pages, including claims 1-67 & Abstract)
- 6. Executed Declaration
- 7. 4 sheets of formal drawings (Figs. 1-7)
- 8. Assignment w/Recordation Cover Sheet

Large Entity Status [x] Small Entity Status []

The Commissioner is hereby authorized to charge payment of fees or credit overpayments to Deposit Account No. 12-0769 in connection with any patent application filing fees under 37 CFR 1.16, and any processing fees under 37 CFR 1.17.

Date: 11/7/00
By: Daniel L. Hayes
Daniel L. Hayes
Reg. No. 34,618

CERTIFICATE OF MAILING

I hereby certify that the items listed above as enclosed are being deposited with the U.S. Postal Service as either first class mail, or Express Mail if the blank for Express Mail No. is completed below, in an envelope addressed to The Commissioner of Patents and Trademarks, Washington, D.C. 20231, on the below-indicated date. Any Express Mail No. has also been marked on the listed items.

Express Mail No. (if applicable) EL685270387

Date: Nov. 7, 2000
By: Helen M. Hare
Helen M. Hare

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision

TOTAL AMOUNT OF PAYMENT

(\$)1,916⁰⁰**Complete if Known**

Application Number

Filing Date

First Named Inventor

Sidiropoulos et al.

Examiner Name

Group Art Unit

Attorney Docket No.

RBI-005US**METHOD OF PAYMENT**

- 1.
- ☒
- The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to

Deposit
Account
Number12-0769Deposit
Account
NameLee & Hayes, PLLC

- ☒
- Charge Any Additional Fee Required
-
- Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status.
See 37 CFR 1.27

- 2.
- ☒
- Payment Enclosed:

☒ Check ☐ Credit card ☐ Money
Order ☐ Other**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity Small Entity

Fee Fee Fee Fee Fee Description

Code (\$)	Code (\$)	Code (\$)	Code (\$)	Code (\$)	Fee Description	Fee Paid
101	710	201	355		Utility filing fee	<u>710</u>
106	320	206	160		Design filing fee	
107	490	207	245		Plant filing fee	
108	710	208	355		Reissue filing fee	
114	150	214	75		Provisional filing fee	

SUBTOTAL (1) (\$)710⁰⁰**2. EXTRA CLAIM FEES**

Total Claims	Extra Claims	Fee from below	Fee Paid
<u>67</u>	-20** = <u>47</u>	<u>18</u>	<u>846</u>
Independent Claims	<u>7</u>	-3** = <u>4</u>	<u>320</u>
Multiple Dependent			

Large Entity Small Entity

Fee Fee Fee Fee Fee Description

Code (\$)	Code (\$)	Code (\$)	Code (\$)	Code (\$)	Fee Description	Fee Paid
103	18	203	9		Claims in excess of 20	
102	80	202	40		Independent claims in excess of 3	
104	270	204	135		Multiple dependent claim, if not paid	
109	80	209	40		** Reissue independent claims over original patent	
110	18	210	9		** Reissue claims in excess of 20 and over original patent	

SUBTOTAL (2)

(\$)1166⁰⁰

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity Small Entity

Fee Fee Fee Fee Fee

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Fee Description

Fee Paid

105 130 205 65 Surcharge - late filing fee or oath

127 50 227 25 Surcharge - late provisional filing fee or cover sheet

139 130 139 130 Non-English specification

147 2,520 147 2,520 For filing a request for *ex parte* reexamination

112 920* 112 920* Requesting publication of SIR prior to Examiner action

113 1,840* 113 1,840* Requesting publication of SIR after Examiner action

115 110 215 55 Extension for reply within first month

116 390 216 195 Extension for reply within second month

117 890 217 445 Extension for reply within third month

118 1,390 218 695 Extension for reply within fourth month

128 1,890 228 945 Extension for reply within fifth month

119 310 219 155 Notice of Appeal

120 310 220 155 Filing a brief in support of an appeal

121 270 221 135 Request for oral hearing

138 1,510 138 1,510 Petition to institute a public use proceeding

140 110 240 55 Petition to revive - unavoidable

141 1,240 241 620 Petition to revive - unintentional

142 1,240 242 620 Utility issue fee (or reissue)

143 440 243 220 Design issue fee

144 600 244 300 Plant issue fee

122 130 122 130 Petitions to the Commissioner

123 50 123 50 Petitions related to provisional applications

126 240 126 240 Submission of Information Disclosure Stmt

581 40 581 40 Recording each patent assignment per property (times number of properties)

146 710 246 355 Filing a submission after final rejection (37 CFR § 1.129(a))

149 710 249 355 For each additional invention to be examined (37 CFR § 1.129(b))

179 710 279 355 Request for Continued Examination (RCE)

169 900 169 900 Request for expedited examination of a design application

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3)

(\$)40⁰⁰**SUBMITTED BY**

Name (Print/Type)

Daniel L. HayesRegistration No.
(Attorney/Agent)34,618

Complete (if applicable)

Telephone

(509) 324-9256

Signature

Daniel L. Hayes

Date

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

**Reducing Coupled Noise in Pseudo-Differential
Signaling Systems**

Inventors:

Stefanos Sidiropoulos

Ying Li

Mark A. Horowitz

ATTORNEY'S DOCKET NO. RB1-005US

TECHNICAL FIELD

The present invention relates to the transmission of data over transmission lines that are subject to capacitively and/or inductively coupled noise. More specifically, the present invention reduces the effect of such induced or coupled noise in systems using pseudo-differential transmission lines.

BACKGROUND

Fig. 1 shows an electronic system that transmits data or other signals using pseudo-differential signaling. The system includes a first integrated circuit 10 that transmits the signals, and a second integrated circuit 12 that receives the signals. The signals comprise voltages that are conducted between the two integrated circuits by a plurality of signal lines 14. The signal lines are typically metallic traces on a printed circuit board.

In addition to the signals themselves, a reference voltage is transmitted from first integrated circuit 10 to second integrated circuit 12, over a reference line 16. The signal voltages represent values in terms of relationships between the signal voltages and the reference voltage. In a binary system, for example, a high voltage—one which is higher than the reference voltage—might represent a binary “1”. A low voltage—one that is less than the reference voltage—might represent a binary “0”.

Fig. 2 illustrates how the values of signal lines are determined within the receiving integrated circuit 12. A signal comparator 20, often in the form of a comparator, is associated with each signal voltage V_{SIG} . Each signal line is routed to a first input of the associated signal comparator 20. The reference voltage V_{REF} is routed in common to the second input of each signal comparator 20. The signal

1 comparator produces a high logic level within integrated circuit 12 if the signal
2 voltage is higher than the reference voltage. The signal comparator produces a
3 low logic level within integrated circuit 12 if the signal voltage is not higher than
4 the reference voltage.

5 This type of signaling technique reduces or cancels the effect of any
6 electrical noise that is induced in signal lines 14 between the two integrated
7 circuits. The technique works on the assumption that any noise induced in a signal
8 line will be similarly induced in the common reference line. This assumption, in
9 turn, relies on the further assumption that the signal lines are subject to the same
10 noise inducing influences as the reference line.

11 These assumptions are generally correct, at least to a degree. In high-speed
12 data transfer circuits, however, it is often desired to utilize very small differentials
13 between "high" and "low" signal voltages. The use of such small voltage
14 differentials accentuates the effect of any differences in induced noise between the
15 signal lines and the reference line.

16 In sensitive circuits such as these, even small differences in induced noise
17 can become significant. One reason such differences arise is that the reference
18 line is routed to many more components than an individual signal line.
19 Specifically, a signal line is routed (within the receiving integrated circuit) to only
20 a single signal comparator. The reference line, on the other hand, is routed to all
21 of the signal comparators. Each connection to signal comparator introduces a new
22 source of noise coupling. Furthermore, additional routing lengths are usually
23 required to reach the signal comparators, which also adds coupling capacitance.

24 Fig. 3 shows a simplified model of a reference line 30 and a signal line 32.
25 The lines are driven by devices having equal output impedances, and the

transmission lines are carefully designed to have the same distributed line impedances. The transmission line and driver impedances are represented as R_C in Fig. 3.

At the receiving integrated circuit, the reference line and signal line are connected to a package pin. This pin introduces a parasitic inductance L_I . Within the integrated circuit, both of the lines are capacitively coupled to the substrate (V_{SS}) of the integrated circuit. This coupling is mainly through the capacitances of the input pad, existing electrostatic discharge (ESD) circuitry, and the inputs of the signal comparators. Since the reference line drives a multitude of signal comparators and has a longer routing path, its coupling capacitance C_{REF} is significantly larger than the capacitance C_{IN} of the signal line. Moreover, depending on the length and the resistivity of the reference routing wire, the additional capacitance of the reference line may behave as a distributed RC line.

The capacitive coupling C_{REF} and C_{IN} result in noise injection from the integrated circuit's power supply rails to the signal and reference lines. If C_{REF} and C_{IN} were equal, the noise injection would be common mode and would not affect the interpretation of the signal. But because C_{REF} is so much greater than C_{IN} in a pseudo-differential interface, the noise injection on the reference line is fundamentally larger than that on the signal line. This results in a reduction of common mode noise rejection by the signal comparators, especially at high frequencies.

The technique described below reduces the effect of noise injection in pseudo-differential interfaces such as shown in Figs. 1-3.

SUMMARY

In the circuits described below, the reference voltage is buffered in the receiving circuit prior to its distribution to the multiple signal comparators. In one embodiment, the buffered voltage is the sum of the reference voltage and its noise. In another embodiment, the buffered voltage represents only the noise.

The buffered voltage is used in each embodiment to account for the differences between impedances seen by the signal voltages and the relatively greater impedances seen by the reference voltage.

In one embodiment, the buffering is accomplished with an active buffer such as a unity gain operational amplifier, having a bandwidth that is significantly greater than the resonant input frequency of the reference and signal inputs.

Alternatively, both the signal voltages and the reference voltages are buffered using MOSFET source-followers. To reduce differential noise injection, the source-follower associated with the reference input is larger than the source-follower of the signal inputs by specific ratio. This ratio is equal to the ratio of the capacitance seen by the output of the source-follower associated with the reference line to the capacitance seen by the output of the source-follower associated with the signal line.

In another embodiment, the buffered voltage represents only the noise of the signal lines, and is subtracted from the signal voltages to remove the noise.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a prior art pseudo-differential signaling system.

Fig. 2 illustrates receiving circuitry of a prior art pseudo-differential signaling system.

Fig. 3 illustrates electrical characteristics of signal and reference lines in a prior art pseudo-differential signaling system.

Fig. 4 illustrates a pseudo-differential signaling system in which the invention can be embodied.

Fig. 5 illustrates electrical characteristics of a receiving circuit in a pseudo-differential signaling system.

Figs. 6 and 7 illustrate electrical characteristics of receiving circuits in alternative embodiments of pseudo-differential signaling systems.

DETAILED DESCRIPTION

Fig. 4 shows a system 100 including a first integrated circuit 102 that transmits pseudo-differential data signals in conjunction with a reference signal, and a second integrated circuit 104 that receives the data and reference signals. Specifically, the signals include a plurality of pseudo-differential data signal voltages, referred to herein simply as signal voltages, and a single, common reference voltage. These signals are conducted on corresponding pseudo-differential signal lines 106 and a reference line 108.

The pseudo-differential data signals represent values in terms of relationships between the signal voltages and the common reference voltage. In the described embodiment, for example, a signal voltage that is higher than the reference voltage represents a binary "1". A data signal voltage that is lower than the reference voltage represents a binary "0".

Fig. 5 shows receiver circuitry, within receiving integrated circuit 104, corresponding to the reference signal and one of the signal lines. Parasitic inductance L_1 is introduced on each signal line by the corresponding package pins

on the integrated circuit—the external pins to which the lines are routed from the transmitting integrated circuit.

Each signal line is routed within integrated circuit 104 to a signal receiver or comparator 110. Integrated circuit 104 has a plurality of such signal comparators, corresponding respectively to each of the received pseudo-differential signals.

With regard to the data signal lines, coupling capacitance is represented as C_S . Noise is injected into each data signal line from the integrated circuit's substrate V_{SS} through coupling capacitance C_S . C_S is a result of capacitances of the input pad corresponding to the signal line, existing ESD circuitry, and the input of the data signal comparator 110.

The reference voltage or signal is routed within the integrated circuit to a reference receiver 112, before the reference voltage has been distributed to the various signal comparators. In this embodiment, the reference receiver is an active buffer. More specifically, reference receiver 112 is a unity gain amplifier—preferably an operational amplifier—that receives the common reference voltage and in response produces a buffered common reference voltage or signal V_{BUF} , also referred to herein as a buffered signal or voltage. The buffered voltage is distributed to each of data signal comparators 110. Thus, each data signal comparator compares or otherwise evaluates the buffered reference voltage and the corresponding pseudo-differential signal voltage to determine the value represented by the signal voltage.

In the described embodiment, each signal comparator comprises a transistor-based comparator that compares two input voltages and produces a

1 binary voltage output that is dependent on which of the two input voltages is
2 greater. Optionally, the voltage output might be produced as a differential signal.

3 With regard to the reference line, coupling capacitance includes C_{R1} and
4 C_{R2} . C_{R1} represents coupling capacitance of the *unbuffered*, undistributed,
5 common reference signal, and is a result of capacitances of the input pad
6 corresponding to the reference line, ESD circuitry, and the input of active buffer
7 112. Noise is injected into the unbuffered reference line from the integrated
8 circuit's substrate V_{SS} through coupling capacitance C_{R1} . Active buffer 112 is
9 designed to have an input capacitance approximately equal to the input
10 capacitance of any one of the data signal comparators 110 and also to equal C_{R1} .
11 This ensures that integrated circuit 104 presents similar input impedances to both
12 the unbuffered reference voltage and the multiple signal voltages.

13 C_{R2} represents coupling capacitance of the *buffered* reference signal. This
14 capacitance is due primarily to the combined capacitances of the inputs of the
15 multiple signal comparators 110. Active buffer 112 is designed with a large
16 enough bandwidth to minimize the effects of C_{R2} and to thereby minimize any
17 noise injection through C_{R2} .

18 In the circuit of Fig. 5, noise induced by capacitive coupling in the
19 receiving integrated circuit will be largely common mode, since C_S equals C_{R1} and
20 since active buffer 112 has a sufficient bandwidth to largely negate any significant
21 noise injection through C_{R2} . In practice, active buffer 112 should have a
22 bandwidth that is significantly greater than the resonant input frequency of the
23 data signal line—a function of L_I and C_S . Specifically, the bandwidth of active
24 buffer 112 should be at least ten times greater than the resonant input frequency of
25 the data signal lines.

1 This circuit arrangement ensures that approximately equal coupled signal
2 noise is introduced in the distributed reference voltage and the plurality of pseudo-
3 differential signal voltages. Such common mode noise is canceled in the
4 comparisons performed by the signal comparators.

5 The described technique has been found to be extremely practical and
6 beneficial, especially in integrated circuits running at higher clock speeds and
7 having higher values of L_1 .

8 Fig. 6 illustrates an alternative embodiment in which both the signal
9 voltages and the reference voltage are buffered. Specifically, the receiving
10 integrated circuit has a plurality of receivers or active buffers 202 that receive the
11 pseudo-differential signal voltages and in response produce buffered signal
12 voltages. Similarly, the reference voltage is routed to a single receiver or active
13 buffer 204 that produces a buffered reference voltage. The buffers need not have a
14 unity gain, but they do have approximately identical gains. In the described
15 embodiment, they are MOSFET-based source-followers.

16 Coupling capacitance associated with the signal voltage includes C_{S1} and
17 C_{S2} . C_{S1} represents coupling capacitance of the *unbuffered* signal voltage, and is a
18 result of capacitances of the input pad corresponding to the signal line, ESD
19 circuitry, and the input of the active buffer 202. Noise is injected into the
20 unbuffered signal line from the integrated circuit's substrate V_{SS} through coupling
21 capacitance C_{S1} .

22 C_{S2} represents coupling capacitance of the *buffered* signal voltage. This
23 capacitance is due primarily to the capacitance of the input of a signal comparator
24 210 associated with each signal line.
25

Coupling capacitance associated with the reference voltage includes C_{R1} and C_{R2} . C_{R1} represents coupling capacitance of the *unbuffered*, undistributed reference voltage, and is a result of capacitances of the input pad corresponding to the reference line, ESD circuitry, and the input of the active buffer 204. Noise is injected into the unbuffered reference line from the integrated circuit's substrate V_{SS} through coupling capacitance C_{R1} .

C_{S2} represents coupling capacitance of the *buffered* and distributed reference voltage. This capacitance is due primarily to the capacitance of the input of signal comparator 210.

In this circuit, C_{S1} is approximately equal to C_{R1} . Thus, any noise injected through these capacitances will be common mode. However, C_{R2} is significantly greater than C_{S2} , due to the multitude of signal comparators whose inputs receive the buffered reference voltage. Noise injected through these capacitances tends to contain non-common mode components. However, such non-common mode noise can be greatly reduced by designing the active buffer associated with the reference line with much larger transistors than the active buffers associated with the data signal lines. Specifically, active buffer 204 is designed to have an electrical current capacity that is greater than the electrical current capacity of active buffer 202 by a ratio equal to the ratio of C_{R2} to C_{S2} .

A larger buffer will usually have a higher input capacitance, which will tend to make C_{R1} greater than C_{S1} . However, C_{R1} and C_{S1} are typically dominated by ESD components so that the input capacitances of the active buffers have only negligible effect. Furthermore, the signal line inputs can employ dummy capacitors to equalize C_{R1} and C_{S1} .

Fig. 7 illustrates a third embodiment, appropriate for use in conjunction with two-stage input receivers. This embodiment comprises a plurality of two-stage input receivers 302, and a reference receiver or buffer 304. Input inductance and capacitance are represented in Fig. 7 as L_I and C_I , respectively. The circuit receives a plurality of signal voltages V_{SIGEXT} , which are subject to input inductance L_I and capacitance C_I to produce internal signal voltages referred to as V_{SIG} . The circuit also receives a voltage reference signal V_{REF} , which similarly subject to input inductance L_I and capacitance C_I to produce internal reference voltages referred to as V_{REFU} and V_{REFD} .

The first stage of a two-stage input receiver typically performs signal conditioning such as filtering, translating the input levels from the allowable input common-mode range to a fixed-output common-mode voltage, and converting the single-ended input into a differential output for the second stage. The second stage typically provides gain and performs latching.

In the circuit shown in Fig. 7, a two-stage input receiver 302 is provided for each incoming signal line. A first stage 310 of a receiver receives both a signal voltage V_{SIG} and a distributed reference voltage V_{REFD} . The term “distributed” in this context means that the reference voltage is provided to a plurality of receivers. First stage 310 conditions the signals and determines the voltage differential between them. This voltage differential is then provided to a second stage 312, in the form of a buffered differential voltage V_{BUF1} .

Reference receiver 304 has characteristics similar to first stages 310. Specifically, it has a similar or identical input impedance. In many cases, it is a duplicate of the circuits used within first stages 310.

1 Reference receiver 304 receives the distributed voltage V_{REFD} , and an
2 undistributed voltage V_{REFU} . V_{REFU} is a voltage or signal that has not been
3 distributed to all of the signal receivers. In this embodiment, the undistributed
4 reference voltage is connected to only to the single reference receiver 304.

5 The reference receiver is similar to the first stages 310 of the signal
6 receivers and performs similar functions. Specifically, it produces a buffered
7 differential voltage or signal V_{BUF2} , based on the voltage differential between its
8 two inputs—between V_{REFD} and V_{REFU} .

9 In operation, each V_{SIG} is subject to a load equal to the sum of the signal
10 line impedance (L_I and C_I) and the input impedance of first stage receiver 310.
11 V_{REFD} , however, is additionally subject to a load equal to sum of the signal line
12 impedance (L_I and C_I) and the cumulative input impedance of *all* the first stage
13 receivers 310. Because of this, noise is not produced equally in the distributed
14 reference voltage V_{REFD} as compared to each of the signal voltages V_{SIG} . In other
15 words, the difference between V_{SIG} and V_{REFD} will have a noise component equal
16 to the difference in noise between the signal voltage V_{SIG} and the distributed
17 reference voltage V_{REFD} . V_{REFU} , on the other hand, is subject to the load of only a
18 single receiver 304, just as the signal lines V_{SIG} .

19 The circuit of Fig. 6 works by generating a buffered voltage V_{BUF2} , which is
20 based at least in part on undistributed reference voltage V_{REFU} . Specifically, V_{BUF2}
21 is equal to V_{REFD} minus V_{REFU} : the difference between the relatively unloaded
22 reference voltage V_{REFU} as it is received and the more heavily loaded reference
23 voltage V_{REFD} after it is distributed to all of the input receivers 310. It also
24 represents the difference between the induced noise on V_{SIG} and the averaged
25 induced noise present on V_{REFD} .

1 To produce V_{BUF2} , both V_{REFD} and V_{REFU} are connected to the inputs of
2 reference receiver 304, which compares the two voltages and produces V_{BUF2} .
3 V_{BUF2} is distributed to the second stage 312 of each signal receiver 302. In
4 addition, the second stage receives the voltage produced by the first stage of the
5 signal receiver. To correct for noise, the second stage is configured to subtract
6 V_{BUF1} from V_{BUF2} . This results in a noise-compensated output voltage V_{OUT} .

7 Additional noise and signal degradation in V_{BUF2} are avoided by the use of
8 a differential output from reference receiver 304. First stage 310 also generates a
9 differential output, which avoids additional noise on V_{BUF2} . In addition, receivers
10 304 and 310 produce sampled outputs, so that the bandwidth of the amplifier
11 driving the noise signal is less critical—one can allocate some time for this
12 amplifier to settle.

13 A feature of this embodiment is that the noise (V_{BUF2}) is not distributed as a
14 full amplitude signal, equal to the reference voltage plus the noise. Rather, V_{BUF2}
15 in this embodiment represents only noise, and has much smaller amplitude than
16 the summed amplitude V_{BUF} of the previous embodiments.

17 The circuits described above improve the performance of pseudo-
18 differential signals, allowing smaller voltage differentials to be utilized so that
19 higher switching speeds can be attained.

20 Although the description above uses language that is specific to structural
21 features and/or methodological acts, it is to be understood that the invention
22 defined in the appended claims is not limited to the specific features or acts
23 described. Rather, the specific features and acts are disclosed as exemplary forms
24 of implementing the invention.
25

1 **CLAIMS**

2 1. An apparatus that uses pseudo-differential voltage signaling,
3 comprising:

4 a reference receiver that receives an undistributed reference voltage and in
5 response produces a buffered voltage that is derived at least in part from the
6 undistributed reference voltage;

7 signal receivers associated respectively with a plurality of signal voltages;

8 wherein an individual signal receiver receives both its associated signal
9 voltage and the buffered voltage, and;

10 wherein said individual signal receiver evaluates its associated signal
11 voltage and the buffered voltage to produce an output voltage.

12
13 2. An apparatus as recited in claim 1, wherein said individual signal
14 receiver evaluates by comparing the associated signal voltage and the buffered
15 voltage to produce an output voltage.

16
17 3. An apparatus as recited in claim 1, wherein the buffered voltage is the
18 difference between the undistributed reference voltage and a distributed reference
19 voltage.

20
21 4. An apparatus as recited in claim 1, wherein the buffered voltage is
22 proportional to the undistributed reference voltage.

1 5. An apparatus as recited in claim 1, wherein the buffered voltage
2 represents the noise of the signal voltages relative to the undistributed reference
3 voltage.

4
5 6. An apparatus as recited in claim 1, wherein the reference receiver
6 also receives a distributed reference voltage that is received by the signal
7 receivers, wherein the reference receiver is responsive to the distributed reference
8 voltage and the undistributed reference voltage to produce the buffered voltage.

9
10 7. An apparatus as recited in claim 1, wherein the reference receiver
11 also receives a distributed reference voltage that is received by the signal
12 receivers, wherein the reference receiver compares the distributed reference
13 voltage and the undistributed reference voltage to produce the buffered voltage.

14
15 8. An apparatus as recited in claim 1, wherein the reference receiver
16 also receives a distributed reference voltage that is received by the signal
17 receivers, wherein the reference receiver compares the distributed reference
18 voltage and the undistributed reference voltage to produce the buffered voltage,
19 the buffered voltage representing the difference between the distributed reference
20 voltage and the undistributed reference voltage.

21
22 9. An apparatus as recited in claim 1, further comprising:
23 a plurality of signal buffers that receive the signal voltages and in response
24 produce buffered signal voltages, wherein each buffered signal voltage is subject
25 to a signal capacitance;

1 the buffered voltage being subject to a reference capacitance that is
2 significantly greater than the signal capacitance;
3 each of the signal buffers having a first electrical current capacity;
4 the reference receiver having a second electrical current capacity that is
5 greater than the first electrical current capacity by a ratio equal to the ratio of the
6 reference capacitance to the signal capacitance.

7
8 **10.** An apparatus as recited in claim 1, further comprising:
9 a plurality of signal buffers that receive the signal voltages and in response
10 produce buffered signal voltages, wherein each buffered signal voltage is subject
11 to a signal capacitance;
12 the buffered voltage being subject to a reference capacitance that is
13 significantly greater than the signal capacitance;
14 each of the signal buffers having a first electrical current capacity;
15 the reference receiver having a second electrical current capacity that is
16 greater than the first electrical current capacity by a ratio equal to the ratio of the
17 reference capacitance to the signal capacitance; and
18 wherein the reference receiver and the signal buffers are source-followers.

19
20 **11.** An apparatus as recited in claim 1, further comprising:
21 a plurality of signal buffers that receive the signal voltages and in response
22 produce buffered signal voltages.
23
24
25

1 **12.** An apparatus as recited in claim 1, further comprising:
2 a plurality of signal buffers that receive the signal voltages and in response
3 produce buffered signal voltages;

4 wherein the reference receiver and the signal buffers are source-followers.

5
6 **13.** An apparatus as recited in claim 1, wherein the reference receiver
7 has a unity gain.

8
9 **14.** An apparatus as recited in claim 1, wherein:
10 the signal voltage has associated input capacitance and inductance that
11 result in a resonant input frequency;

12 the reference receiver has a bandwidth that is significantly greater than the
13 resonant input frequency.

14
15 **15.** An apparatus as recited in claim 1, wherein:
16 the signal voltage has associated input capacitance and inductance that
17 result in a resonant input frequency;

18 the reference receiver has a bandwidth of at least ten times the resonant
19 input frequency.

20
21 **16.** An apparatus as recited in claim 1, wherein each signal voltage
22 represents one of two values and the signal receivers compare the buffered voltage
23 and the signal voltages to determine which of the two values is represented by
24 each signal voltage.

1 17. An apparatus as recited in claim 1, the reference voltage and the
2 buffered voltage being subject to similar impedances.

3
4 18. An apparatus as recited in claim 1, the reference voltages and signal
5 voltage being subject to similar impedances, wherein coupled signal noise is
6 introduced approximately equally in the buffered voltage and the plurality of
7 pseudo-differential signal voltages, said approximately equal coupled signal noise
8 being canceled in the evaluation performed by the signal receiver.

9
10 19. An integrated circuit comprising:
11 a reference input that receives a common reference voltage;
12 a plurality of signal inputs configured to receive pseudo-differential signal
13 voltages that represent values in terms of relationships between the pseudo-
14 differential signal voltages and the common reference voltage;
15 a reference buffer that receives the common reference voltage and in
16 response produces a buffered reference voltage;
17 signal comparators associated respectively with the plurality of pseudo-
18 differential signal voltages, each signal comparator comparing the buffered
19 reference voltage and one of the pseudo-differential signal voltages to determine
20 the value represented by said one of the pseudo-differential signal voltages;
21 wherein the reference and signal inputs have similar impedances, coupled
22 signal noise being introduced approximately equally in the buffered reference
23 voltage and the plurality of pseudo-differential signal voltages, said approximately
24 equal coupled signal noise being canceled in the comparison performed by the
25 signal comparators.

1
2 **20.** An integrated circuit as recited in claim 19, further comprising:
3 a plurality of signal buffers that receive the pseudo-differential signal
4 voltages and in response produce buffered signal voltages, wherein each buffered
5 signal voltage is subject to a signal capacitance;
6 the buffered reference voltage being subject to a reference capacitance that
7 is significantly greater than the signal capacitance;
8 each of the signal buffers having a first electrical current capacity;
9 the reference buffer having a second electrical current capacity that is
10 greater than the first electrical current capacity by a ratio equal to the ratio of the
11 reference capacitance to the signal capacitance.

12
13 **21.** An integrated circuit as recited in claim 19, further comprising:
14 a plurality of signal buffers that receive the pseudo-differential signal
15 voltages and in response produce buffered signal voltages, wherein each buffered
16 signal voltage is subject to a signal capacitance;
17 the buffered reference voltage being subject to a reference capacitance that
18 is significantly greater than the signal capacitance;
19 each of the signal buffers having a first electrical current capacity;
20 the reference buffer having a second electrical current capacity that is
21 greater than the first electrical current capacity by a ratio equal to the ratio of the
22 reference capacitance to the signal capacitance; and
23 wherein the reference buffer and the signal buffers are source-followers.

1 **22.** An integrated circuit as recited in claim 19, further comprising:
2 a plurality of signal buffers that receive the pseudo-differential signal
3 voltages and in response produce buffered signal voltages for comparison by the
4 signal comparators.

5
6 **23.** An integrated circuit as recited in claim 19, further comprising:
7 a plurality of signal buffers that receive the pseudo-differential signal
8 voltages and in response produce buffered signal voltages;
9 wherein the reference buffer and the signal buffers are source-followers.

10
11 **24.** An integrated circuit as recited in claim 19, wherein the reference
12 buffer has a unity gain.

13
14 **25.** An integrated circuit as recited in claim 19, wherein:
15 the signal inputs have associated input capacitances and inductances that
16 result in a resonant input frequency;
17 the reference buffer has a bandwidth that is significantly greater than the
18 resonant input frequency.

19
20 **26.** An integrated circuit as recited in claim 19, wherein:
21 the signal input has associated input capacitance and inductance that result
22 in a resonant input frequency;
23 the reference buffer has a bandwidth of at least ten times the resonant input
24 frequency.

1 **27.** An integrated circuit as recited in claim 19, wherein each signal
2 voltage represents one of two values and the signal comparators compare the
3 buffered reference voltage and the signal voltages to determine which of the two
4 values is represented by each signal voltage.

5
6 **28.** An integrated circuit as recited in claim 19, the reference and signal
7 inputs having matching impedances.

8
9 **29.** A system comprising:
10 a first integrated circuit that transmits a common reference voltage and a
11 plurality of pseudo-differential signal voltages, wherein the pseudo-differential
12 signal voltages represent values in terms of relationships between the pseudo-
13 differential signal voltages and the common reference voltage;

14 a second integrated circuit that receives the common reference voltage and
15 the plurality of pseudo-differential signal voltages;

16 the second integrated circuit having a reference buffer that receives the
17 common reference voltage and in response produces a buffered reference voltage;

18 the second integrated circuit having signal comparators associated
19 respectively with the plurality of pseudo-differential signal voltages, each signal
20 comparator comparing the buffered reference voltage and a respective one of the
21 pseudo-differential signal voltages to determine the value represented by said one
22 of the pseudo-differential signal voltages;

23 wherein the second integrated circuit is configured to introduce
24 approximately equal coupled signal noise in the buffered reference voltage and the
25 plurality of pseudo-differential signal voltages, said approximately equal coupled

1 signal noise being canceled in the comparisons performed by the signal
2 comparators.

3
4 **30.** A system as recited in claim 29, the second integrated circuit further
5 comprising:

6 a plurality of signal buffers that receive the pseudo-differential signal
7 voltages and in response produce buffered signal voltages, wherein each buffered
8 signal voltage is subject in the second integrated circuit to a signal capacitance;

9 the buffered reference voltage being subject in the second integrated circuit
10 to a reference capacitance that is significantly greater than the signal capacitance;

11 each of the signal buffers having a first electrical current capacity;

12 the reference buffer having a second electrical current capacity that is
13 greater than the first electrical current capacity by a ratio equal to the ratio of the
14 reference capacitance to the signal capacitance.

15
16 **31.** A system as recited in claim 29, the second integrated circuit further
17 comprising:

18 a plurality of signal buffers that receive the pseudo-differential signal
19 voltages and in response produce buffered signal voltages, wherein each buffered
20 signal voltage is subject in the second integrated circuit to a signal capacitance;

21 the buffered reference voltage being subject in the second integrated circuit
22 to a reference capacitance that is significantly greater than the signal capacitance;

23 each of the signal buffers having a first electrical current capacity;
24
25

1 the reference buffer having a second electrical current capacity that is
2 greater than the first electrical current capacity by a ratio equal to the ratio of the
3 reference capacitance to the signal capacitance; and

4 wherein the reference buffer and the signal buffers are source-followers.

5
6 **32.** A system as recited in claim 29, the second integrated circuit further
7 comprising:

8 a plurality of signal buffers that receive the pseudo-differential signal
9 voltages and in response produce buffered signal voltages.

10
11 **33.** A system as recited in claim 29, the second integrated circuit further
12 comprising:

13 a plurality of signal buffers that receive the pseudo-differential signal
14 voltages and in response produce buffered signal voltages;

15 wherein the reference buffer and the signal buffers are source-followers.

16
17 **34.** A system as recited in claim 29, wherein the reference buffer is a
18 unity gain amplifier.

19
20 **35.** A system as recited in claim 29, wherein:
21 the second integrated circuit has signal inputs that receive the plurality of
22 signal voltages, the signal inputs having associated input capacitance and
23 inductance that result in a resonant input frequency;
24 the reference buffer has a bandwidth that is significantly greater than the
25 resonant input frequency.

1
2 **36.** A system as recited in claim 29, wherein:
3 the second integrated circuit has signal inputs that receive the plurality of
4 signal voltages, the signal inputs having associated input capacitance and
5 inductance that result in a resonant input frequency;

6 the reference buffer has a bandwidth of at least ten times the resonant input
7 frequency.
8

9 **37.** A system as recited in claim 29, wherein each pseudo-differential
10 signal voltage represents one of two values and the comparators compare the
11 buffered reference voltage and the pseudo-differential signal voltages to determine
12 which of the two values is represented by each pseudo-differential signal voltage.
13

14 **38.** A system as recited in claim 29, wherein the second integrated
15 circuit has signal inputs that receive the pseudo-differential signal voltages and a
16 reference input that receives the common reference voltage, the reference and
17 signal inputs having similar impedances.
18

19 **39.** A method comprising:
20 receiving a reference voltage;
21 receiving a plurality of signal voltages;
22 producing a buffered voltage based at least in part on the reference voltage;
23 evaluating the buffered voltage and one of the signal voltages to determine
24 a value represented by said one of the signal voltages.
25

1 **40.** A method as recited in claim 39, wherein the evaluating comprises
2 comparing said one of the signal voltages and the buffered voltage to produce an
3 output voltage.

4
5 **41.** A method as recited in claim 39, wherein the buffered voltage is the
6 difference between an undistributed reference voltage and a distributed reference
7 voltage.

8
9 **42.** A method as recited in claim 39, wherein the buffered voltage is
10 proportional to the reference voltage.

11
12 **43.** A method as recited in claim 39, wherein the buffered voltage
13 represents the noise of the signal voltages.

14
15 **44.** A method as recited in claim 39, said producing comprising
16 comparing a distributed reference voltage that is received by the signal receivers
17 and an undistributed reference voltage that is not received by the signal receivers.

18
19 **45.** A method as recited in claim 39, said producing comprising
20 comparing a distributed reference voltage that is received by the signal receivers
21 and a undistributed reference voltage that is not received by the signal receivers,
22 the buffered voltage representing the difference between the undistributed
23 reference voltage and the distributed reference voltage.

1 **46.** A method as recited in claim 39, further comprising:
2 buffering the signal voltages with signal buffers to produce buffered signal
3 voltages, wherein each buffered signal voltage is subject to a signal capacitance;
4 said producing the buffered voltage being performed with a reference
5 buffer, the buffered voltage being subject to a reference capacitance that is
6 significantly greater than the signal capacitance;
7 each of the signal buffers having a first electrical current capacity;
8 the reference buffer having a second electrical current capacity that is
9 greater than the first electrical current capacity by a ratio equal to the ratio of the
10 reference capacitance to the signal capacitance.

11
12 **47.** A method as recited in claim 39, further comprising:
13 buffering the signal voltages with source-follower signal buffers to produce
14 buffered signal voltages, wherein each buffered signal voltage is subject to a
15 signal capacitance;
16 said producing the buffered voltage being performed with a source-follower
17 reference buffer, the buffered voltage being subject to a reference capacitance that
18 is significantly greater than the signal capacitance;
19 each of the signal buffers having a first electrical current capacity;
20 the reference buffer having a second electrical current capacity that is
21 greater than the first electrical current capacity by a ratio equal to the ratio of the
22 reference capacitance to the signal capacitance.

23
24 **48.** A method as recited in claim 39, further comprising:
25 buffering the signal voltages to produce buffered signal voltages.

1
2 **49.** A method as recited in claim 39, further comprising:
3 buffering the signal voltages with source-followers to produce buffered
4 signal voltages.

5
6 **50.** A method as recited in claim 39, wherein:
7 the signal voltages are received by signal inputs having associated input
8 capacitances and inductances that define a resonant frequency;
9 producing the buffered voltage with a unity gain buffer having a bandwidth
10 that is significantly greater than the resonant frequency.

11
12 **51.** A method as recited in claim 39, wherein:
13 the signal voltages are received by signal inputs having associated input
14 capacitances and inductances that define a resonant input frequency;
15 producing the buffered voltage with a unity gain buffer having a bandwidth
16 of at least ten times the resonant input frequency.

17
18 **52.** A method as recited in claim 39, wherein:
19 the reference voltage is received by a reference input;
20 the signal voltages are received by signal inputs; and
21 the reference and signal inputs have similar impedances.
22
23
24
25

1 **53.** A method as recited in claim 39, further comprising introducing
2 coupled signal noise approximately equally in the buffered reference voltage and
3 the plurality of signal voltages, said approximately equal coupled signal noise
4 being canceled in the comparing.

5
6 **54.** An apparatus that uses pseudo-differential voltage signaling,
7 comprising:

8 signal receivers associated respectively with a plurality of signal voltages;
9 a reference receiver that receives both an undistributed reference voltage
10 and a distributed reference voltage, wherein the distributed reference voltage is
11 distributed to the signal receivers and the undistributed reference voltage is not
12 distributed to the signal receivers;

13 wherein the reference receiver evaluates the undistributed reference voltage
14 and the distributed reference voltage to produce a buffered voltage that represents
15 the difference between the undistributed reference voltage and the distributed
16 reference voltage;

17 wherein an individual signal receiver receives both its associated signal
18 voltage and the buffered voltage; and

19 wherein said individual signal receiver adjusts its associated signal voltage
20 by the buffered voltage to produce an output voltage.

21
22 **55.** An apparatus as recited in claim 54, wherein said signal receivers
23 are two-stage receivers.

1 **56.** An apparatus as recited in claim 54, wherein said signal receivers
2 are two-stage receivers, the second stage of the receivers adjusting the signal
3 voltages.

4
5 **57.** An apparatus as recited in claim 54, wherein the buffered voltage
6 represents the noise of the signal voltages relative to the undistributed reference
7 voltage.

8
9 **58.** An apparatus as recited in claim 54, wherein the buffered voltage is
10 a differential voltage.

11
12 **59.** An integrated circuit that uses pseudo-differential voltage signaling,
13 comprising:

14 two-stage receivers associated respectively with a plurality of signal
15 voltages;

16 a reference receiver that receives both an undistributed reference voltage
17 and a distributed reference voltage, wherein the distributed reference voltage is
18 distributed to the signal receivers and the undistributed reference voltage is not
19 distributed to the signal receivers;

20 wherein the reference receiver compares the undistributed reference voltage
21 and the distributed reference voltage to produce a buffered voltage that represents
22 the difference between the undistributed reference voltage and the distributed
23 reference voltage;

1 wherein the first stage of an individual signal receiver compares its
2 associated signal voltage to the distributed reference voltage to produce a voltage
3 differential signal; and

4 wherein the second stage of said individual two-stage receiver adjusts the
5 voltage differential signal by the buffered voltage to produce an output voltage.

6
7 **60.** An apparatus as recited in claim 59, the two-stage receiver has an
8 input impedance similar to that of the reference receiver.

9
10 **61.** An apparatus as recited in claim 59, wherein the buffered voltage
11 represents the noise of the signal voltages relative to the undistributed reference
12 voltage.

13
14 **62.** An apparatus as recited in claim 59, wherein the buffered voltage is
15 a differential voltage.

16
17 **63.** A system comprising:
18 a first integrated circuit that transmits a common reference voltage and a
19 plurality of pseudo-differential signal voltages, wherein the pseudo-differential
20 signal voltages represent values in terms of relationships between the pseudo-
21 differential signal voltages and the common reference voltage;

22 a second integrated circuit that receives the common reference voltage and
23 the plurality of pseudo-differential signal voltages;

24 the second integrated circuit having a reference receiver that receives the
25 common reference voltage and in response produces a buffered voltage;

1 the second integrated circuit having two-stage signal receivers associated
2 respectively with the plurality of pseudo-differential signal voltages, each two-
3 stage signal receiver adjusting one of the pseudo-differential signal voltages by the
4 buffered voltage to produce an output voltage.

5
6 **64.** A system as recited in claim 63, wherein each two-stage signal
7 receiver has an input impedance similar to that of the reference receiver.

8
9 **65.** A system as recited in claim 63, wherein:
10 the reference receiver compares a distributed common reference voltage to
11 an undistributed common reference voltage to produce the buffered voltage;
12 the first stage of an individual two-stage signal receiver compares its
13 associated pseudo-differential signal voltage to a distributed reference voltage to
14 produce a voltage differential signal; and
15 the second stage of said individual two-stage signal receiver adjusts the
16 voltage differential signal by the buffered voltage to produce an output voltage.

17
18 **66.** A system as recited in claim 63, wherein the buffered voltage
19 represents the noise of the signal voltages.

20
21 **67.** A system as recited in claim 63, wherein the buffered voltage is a
22 differential voltage.
23
24
25

1 **ABSTRACT**

2 A pseudo-differential signaling system uses a plurality of signal lines and a
3 single, common reference voltage. Signal line voltages are interpreted only in
4 comparison to the reference line voltage. Within a receiving circuit, the reference
5 line is buffered prior to its distribution to multiple comparators. The system
6 utilizes an active buffer having a bandwidth that is significantly greater than the
7 resonant input frequency of the receiving circuit. In an alternative embodiment,
8 the signal lines are also buffered. In this embodiment, the buffers are
9 implemented with transistor-based source-followers. The buffer associated with
10 the reference line has a larger current capacity than the buffers associated with the
11 signal lines. In yet another embodiment, a comparator produces a correction
12 signal that is equal to the noise present on the signal lines. This noise is then
13 subtracted from the signal voltages.

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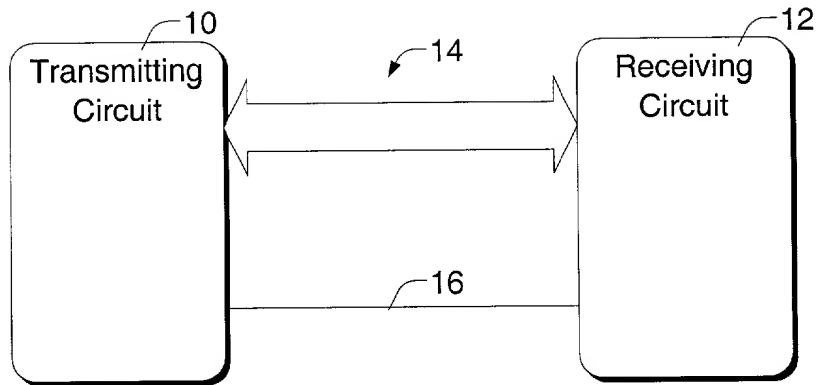


Fig. 1
Prior Art

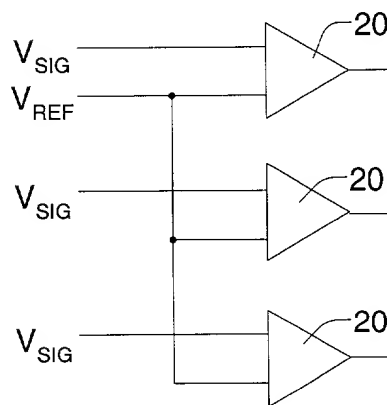


Fig. 2
Prior Art

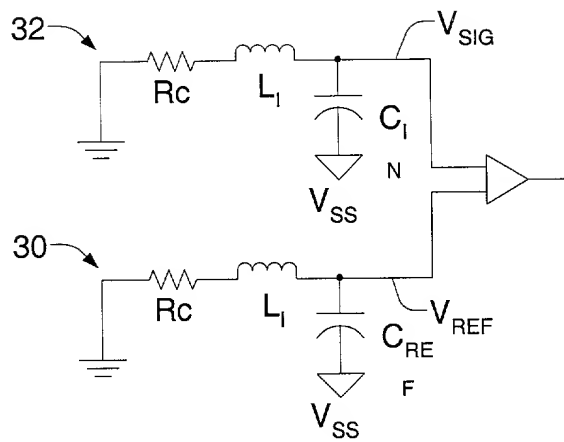


Fig. 3

Prior Art

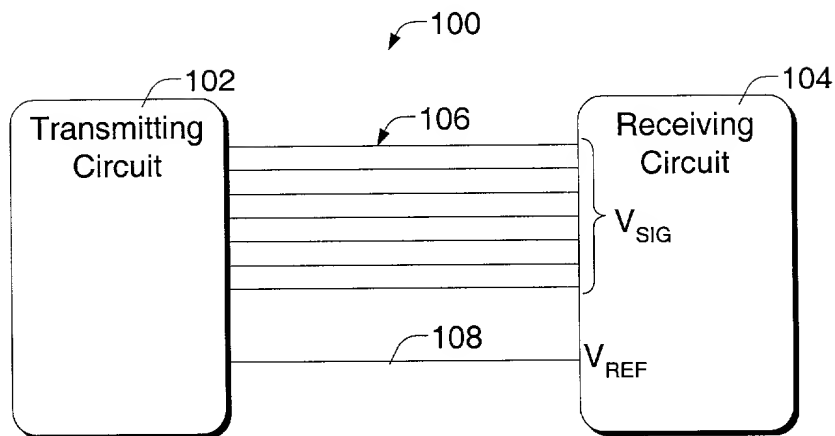


Fig. 4

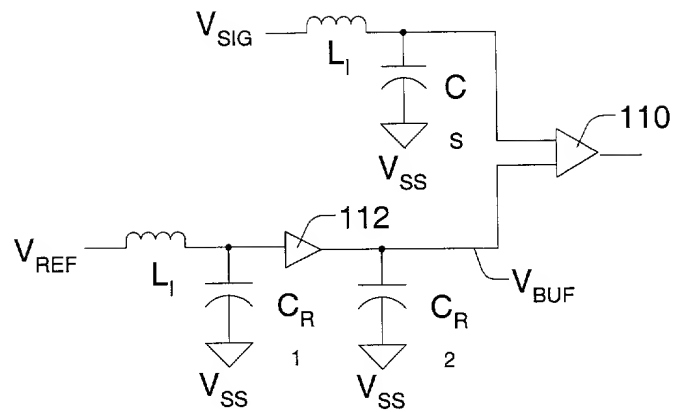


Fig. 5

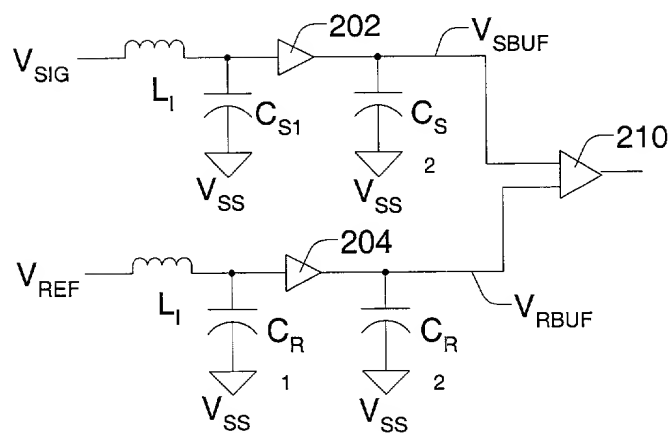


Fig. 6

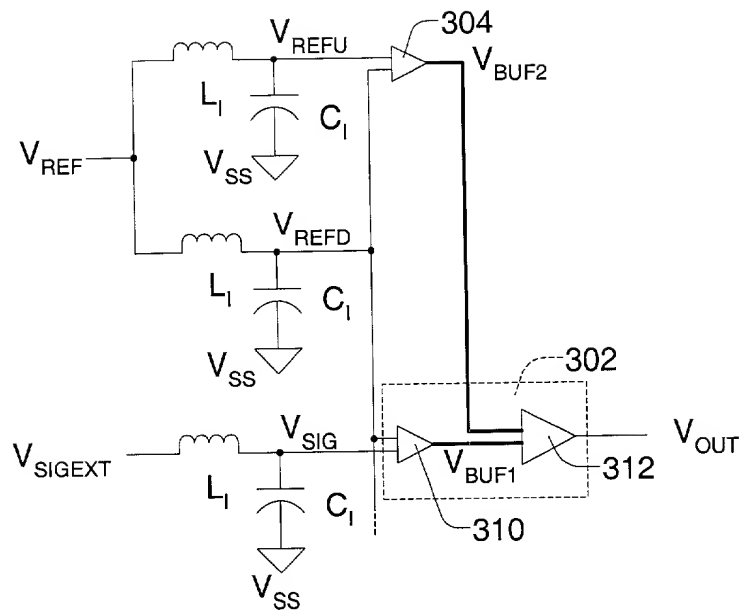


Fig. 7

1 **IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

2 Inventorship Sidiropoulos et al.
3 Applicant..... Rambus Inc.
4 Attorney's Docket No. RB1-005US
5 Title: Reducing Coupled Noise in Pseudo-Differential Signaling Systems

6 **DECLARATION FOR PATENT APPLICATION**

7 As a below named inventor, I hereby declare that:

8 My residence, post office address and citizenship are as stated below next to
9 my name.

10 I believe I am the original, first and sole inventor (if only one name is listed
11 below) or an original, first and joint inventor (if plural names are listed below) of the
12 subject matter which is claimed and for which a patent is sought on the invention
13 entitled "Reducing Coupled Noise in Pseudo-Differential Signaling Systems," the
14 specification of which is attached hereto.

15 I have reviewed and understand the content of the above-identified
16 specification, including the claims.

17 I acknowledge the duty to disclose information which is material to the
18 examination of this application in accordance with Title 37, Code of Federal
19 Regulations, § 1.56(a).

20 PRIOR FOREIGN APPLICATIONS: no applications for foreign patents or
21 inventor's certificates have been filed prior to the date of execution of this
22 declaration.

23 **Power of Attorney**

24 I appoint the following attorneys to prosecute this application and transact all
25 future business in the Patent and Trademark Office connected with this application:
26 Lewis C. Lee, Reg. No. 34,656; Daniel L. Hayes, Reg. No. 34,618; Allan T.

1 Sponseller, Reg. 38,318; Steven R. Sponseller, Reg. No. 39,384; James R.
2 Banowsky, Reg. No. 37,773; Lance R. Sadler, Reg. No. 38,605; Michael A. Proksch,
3 Reg. No. 43,021; Thomas A. Jolly, Reg. No. 39,241; Kasey C. Christie, Reg. No.
4 40,559 and David A. Morasch, Reg. No. 42,905.

5 Send correspondence to: LEE & HAYES, PLLC, 421 W. Riverside Avenue,
6 Suite 500, Spokane, Washington, 99201. Direct telephone calls to: Daniel L. Hayes
7 (509) 324-9256.

8
9 All statements made herein of my own knowledge are true and that all
10 statements made on information and belief are believed to be true; and further that
11 these statements were made with the knowledge that willful false statements and the
12 like so made are punishable by fine or imprisonment, or both, under Section 1001 of
13 Title 18 of the United States Code and that such willful false statement may
14 jeopardize the validity of the application or any patent issued therefrom.

15
16 * * * * *

17 Full name of inventor: Stefanos Sidiropoulos

18 Inventor's Signature



Date: 11/6/2000

19 Residence:

Palo Alto, CA

20 Citizenship:

Greece

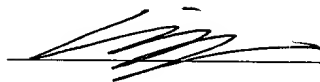
21 Post Office Address:

731 Ellsworth Street
Palo Alto, CA 94306

Full name of inventor:

Yingxuan Li

Inventor's Signature



Date: 11/6/00

Residence:

Cupertino, CA

Citizenship:

China

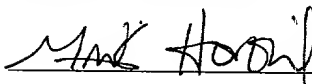
Post Office Address:

902 Cottonwood Drive
Cupertino, CA 95014

Full name of inventor:

Mark A. Horowitz

Inventor's Signature



Date: Nov 3, 2000

Residence:

Menlo Park, CA

Citizenship:

USA

Post Office Address:

1309 San Mateo Drive
Menlo Park, CA 94025